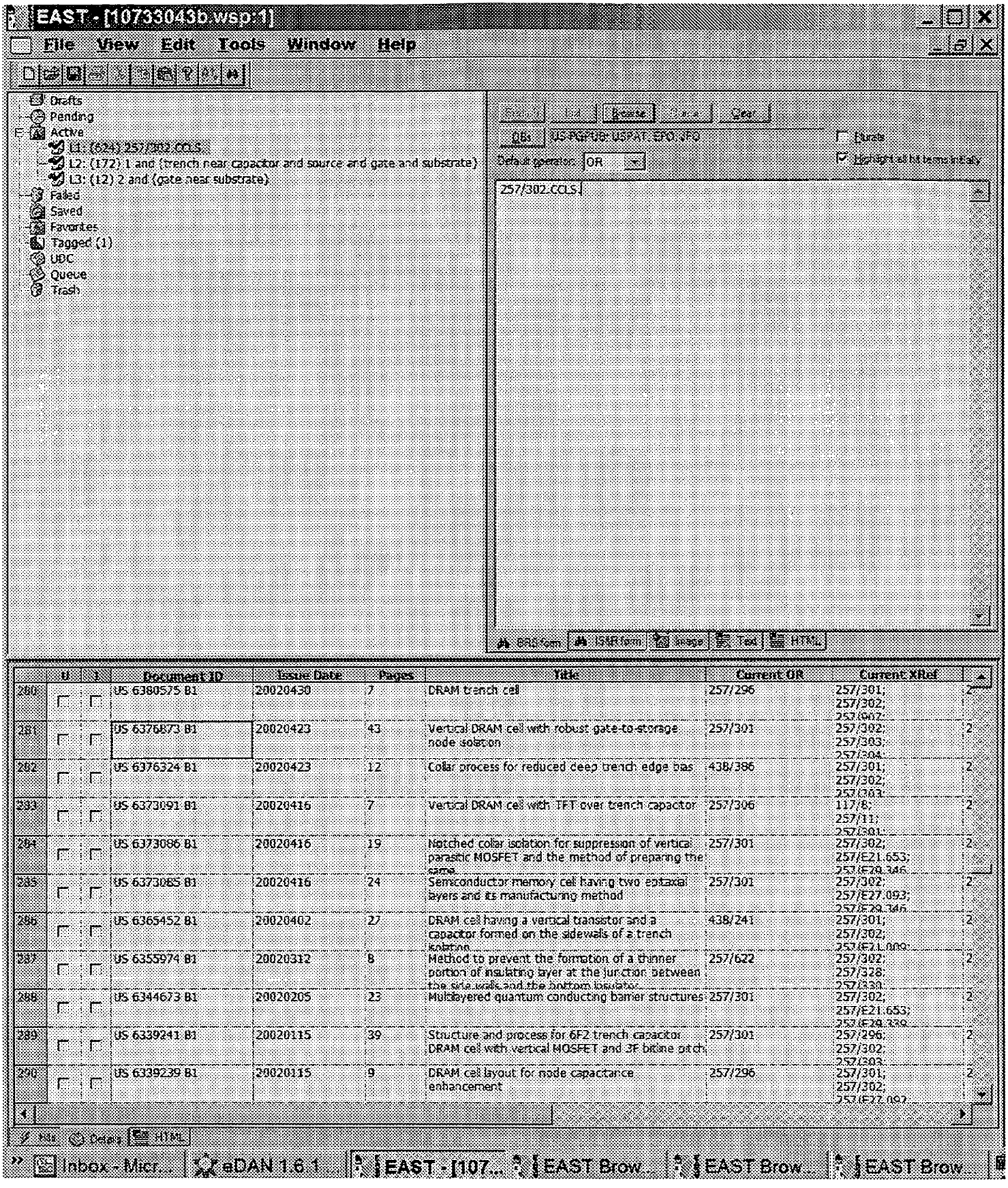
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280 US 6380575 B1 20020430 7 DRAM trench cell 257/296 257/301; 257/302;
281 US 6376873 B1 20020423 43 Vertical DRAM cell with robust gate-to-storage node isolation 257/301 257/302; 257/303;
282 US 6376324 B1 20020423 12 Collar process for reduced deep trench edge bias 438/386 257/301; 257/302;
283 US 6373091 B1 20020416 7 Vertical DRAM cell with TFT over trench capacitor 257/306 117/8; 257/11;
284 US 6373086 B1 20020416 19 Notched collar isolation for suppression of vertical parasitic MOSFET and the method of preparing the same 257/301 257/302; 257/E21.653;
285 US 6373085 B1 20020416 24 Semiconductor memory cell having two epitaxial layers and its manufacturing method 257/301 257/302; 257/E27.093;
286 US 6365452 B1 20020402 27 DRAM cell having a vertical transistor and a capacitor formed on the sidewalls of a trench isolation 438/241 257/301; 257/302;
287 US 6355974 B1 20020312 8 Method to prevent the formation of a thinner portion of insulating layer at the junction between the side walls and the bottom insulator 257/622 257/302; 257/328;
288 US 6344673 B1 20020205 23 Multilayered quantum conducting barrier structures 257/301 257/302; 257/E21.653;
289 US 6339241 B1 20020115 39 Structure and process for 6F2 trench capacitor DRAM cell with vertical MOSFET and 3F bitline pitch 257/301 257/296; 257/302;
290 US 6339239 B1 20020115 9 DRAM cell layout for node capacitance enhancement 257/296 257/301; 257/302;
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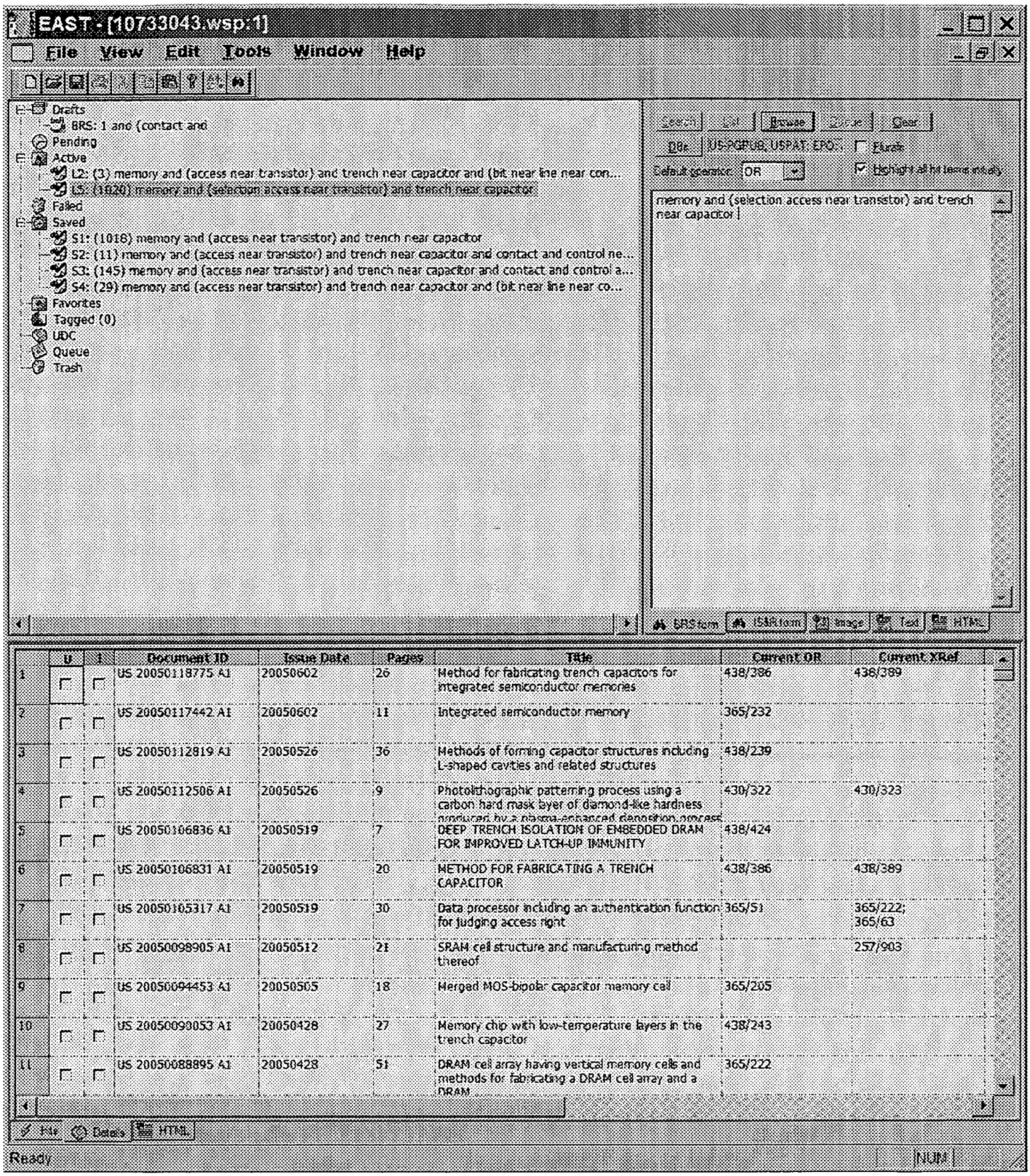
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1 US 20050118775 A1 20050602 26 Method for fabricating trench capacitors for integrated semiconductor memories 438/386 438/389
2 US 20050117442 A1 20050602 11 Integrated semiconductor memory 365/232
3 US 20050112819 A1 20050526 36 Methods of forming capacitor structures including L-shaped cavities and related structures 438/239
4 US 20050112506 A1 20050526 9 Photolithographic patterning process using a carbon hard mask layer of diamond-like hardness produced by a plasma-enhanced deposition process 430/322 430/323
5 US 20050106836 A1 20050519 7 DEEP TRENCH ISOLATION OF EMBEDDED DRAM FOR IMPROVED LATCH-UP IMMUNITY 438/424
6 US 20050106831 A1 20050519 20 METHOD FOR FABRICATING A TRENCH CAPACITOR 438/386 438/389
7 US 20050105317 A1 20050519 30 Data processor including an authentication function for judging access right 365/51 365/222; 365/63
8 US 20050098905 A1 20050512 21 SRAM cell structure and manufacturing method thereof 257/903
9 US 20050094453 A1 20050505 18 Merged MOS-bipolar capacitor memory cell 365/205
10 US 20050090053 A1 20050428 27 Memory chip with low-temperature layers in the trench capacitor 438/243
11 US 20050088895 A1 20050428 51 DRAM cell array having vertical memory cells and methods for fabricating a DRAM cell array and a DRAM 365/222
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